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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/458,551	12/09/1999	ALEXANDER JOFFE	M-5648-ID-US	8981

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EXAMINER	
BANANKHAH, MAJID A	

ART UNIT	PAPER NUMBER
2127	12

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/458,551	Applicant(s) JOFFE ET AL.	
	Examiner Majid A Banankhah	Art Unit 2127	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 1999*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *11-13* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3, 5, 7*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This action is in response to amendment B, paper number 11, response to election restriction, dated January 15, 2004. Claims 1-29 were pending. Claims 1-10 have been cancelled in preliminary amendment dated December 9, 1999. Claims 14-29 are being elected in the response and amendment B, dated January 15, 2004, in response to the restriction requirement filed on may 15, 2003 (paper number 10).

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 14-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Per claim 14, the claim recites: "a processor for executing instructions such that when the processor execute a first instruction accessing an unavailable resource" is indefinite, because, it is unclear as to whether while the instruction is being executed, the processor is accessing an unavailable resource" or the processor is executing, the instruction is accessing an unavailable resource. Additionally, in the line 5-7, the statement "and the processor circuitry which was to execute the first instruction" makes no sense because; in the 2nd line the processor is executes the first instruction. It is unclear what does "which was to execute" means?

Claims 15-17 are rejected for the rejection of their parent claim.

Claims 15, and 24 is rejected because, Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of

elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the step between suspending the first instruction and executing the first instruction. It is unclear as to what steps the processor is taking in regard to first instruction to go to other instructions for processing, while the first instruction is suspended, and when the resource is available, what step does the processor takes to go back to the first instruction.

Claim 16 is so vague that it does not permit understanding of the limitation. The instruction is suspended in claim 1, and now cancelled, still we can re-execute the instruction again when the resource is available. How it is possible to cancel an instruction (say the memory is cleared and there is no place to hold the instruction) and re-execute the instruction back again.

In claim 18, on page 80, in lines 4-7 recites: "and if another task TA2 is ready for execution in place of the task TA1 when the resource is unavailable for the task TA1, the task scheduling circuitry schedule the task TA1". How it is possible, while a task is crippled by not having available resource, and while it is unclear as to when the resource is going to be available, one can schedule the very same task for execution?

Independent claims 19, and 26 has the same problem, claim is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the relationship between the first means (first circuitry) and the second means (second circuitry). The claim is so vague that it does not permit understanding of the limitations or their functions. A first task is suspended, and other tasks are scheduled because of the suspension of the first task.

Claims 20-22, and 27-29 are rejected for the rejection of their parent claims respectively.

Claim 22 is vague because, it is unclear as to which task's is being scheduled while the second circuitry is scheduling the instruction. Its own task or another tasks instruction.

Claims 23-24 is rejected for the same reasons discussed in the rejection of claims 14-15.

Claim 25 is rejected because the relationship between task and instruction is unclear. The statement: "execution of the one or more other instructions comprises execution of one or more other tasks" is vague. It is unclear as to execution of "one instruction" (in the alternative language, the one is considered) can comprises execution of other tasks.

Claim 29 is so vague that it does not permit understanding of the limitation. In lines 1-2, "scheduling **a task** or tasks for execution is performed on each instruction executed by any **one of the tasks"**. Here, scheduling **a task** (in the alternative language, the Examiner choose a task) is performed on each instruction executed by **any one of the tasks**. This does not make sense. Later, "whenever an instruction is to be executed, the task scheduling is performed to schedule a task that will execute the instruction". Here, before the instruction is executed, the scheduling is performed to schedule a task. In the first "quotation" the instruction was executing "Instruction executed by one of the tasks", and here before the instruction was executed scheduling is being performed.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 14-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Okin et. al. (U.S.Pat., No. 6,243,735).

> **While claims 14-29 were rejected under 35 USC 112, second paragraph** as stated above (Section 2-3, *supra*), in order to advance prosecution, claims will be treated on the merits in view of examiner's best understanding of the disclosure and the prior art.

Per claims 14 and 23, the reference of Okin al. teaches of:

a processor for executing instructions such that when the processor executes a first instruction accessing an unavailable resource (col. 1, lines 32-39, *An instruction stream is a sequence of instructions executed by the processor to accomplish a given process, such as add or divide. To date, a processor does either one of the following two things when it encounters* ***a cache miss*** *in an instruction stream: (1) it stays idle until the instruction or data access to the main memory completes, or (2) it executes other instructions in the stream out of order*), the processor suspends the first instruction and the processor circuitry which was to execute the first instruction becomes operable to execute one or more other instructions (*col. 2, lines 29-36, Having multiple copies of state elements on the processor and coupling them to a multiplexer permits the processor* ***to save the context of the current instructions*** *and* ***resume executing new instructions within one clock cycle***). Regarding the phrase "suspending the firs instruction", since the context of the instruction is saved the instruction inherently suspended.

Per claims 15 and 24 wherein the processor executes the first instruction to completion when the resource becomes available (col. 2, lines 13-18, *Should the second process encounters another cache miss, the processor may return within one clock cycle to finish executing the first process if the necessary data had been retrieved from the main memory. Otherwise, the processor may begin executing a third process*).

Per claim 16, wherein when the first instruction becomes suspended, the first instruction is canceled, and the first instruction is re-executed when the resource becomes available (col. 3, lines 34-32, *As such, when a cache miss occurs, the pipeline shall switch from one process to another. In the present example, if the pipeline 6 is executing process 8 when a cache miss occurs,* ***the pipeline 6 is switched within one clock cycle to execute process 10 while saving the contents or states of process 8****. Should process 10 encounters a cache miss before the process 8 retrieves the necessary data from the main memory, the pipeline 6 switches within one clock cycle to another process*).

Per claims 17 and 25, wherein the processor performs multi-tasking (col. 1, lines 62-68, *It is quite common to pipeline the instruction and memory operations of fast processors. A pipeline refers to a processor's ability to perform* ***multiple tasks*** *concurrently in the same clock cycle*), and a task executing the first instruction becomes suspended when the first instruction is suspended (col. 3, lines 10-16, *By state elements, the present invention refers to flip-flops and registers on the processor chip which store binary information indicative of the state of a particular process or processes. Such state elements typically comprise of register files, status bits, condition codes, and pre-fetched instructions*), and while the task is suspended the processor circuitry that was to execute the first instruction is operable to execute one or more other tasks (col. 3, lines 34-44, *As such, when a cache miss occurs, the pipeline shall switch from one process to another. In the present example, if the pipeline 6 is executing process 8 when a cache miss occurs, the pipeline 6 is switched within one clock cycle to execute process 10 while saving the contents or states of process 8. Should* ***process 10 encounters a cache miss*** *before the process 8 retrieves the necessary data from the main memory,* ***the pipeline 6 switches within one***

clock cycle to another process. *Through this construction, the context of a plurality of processes 11 may be saved*).

Per claims 18, 19 and 26, a multi-tasking processor comprising task scheduling circuitry, such that when a task TA1 executed by the processor attempts to access an unavailable resource, the task scheduling circuitry suspends the task TA1 at least until the resource becomes available, and if another task TA2 is ready for execution in place of the task TA1 when the resource is unavailable to the task TA1, the task scheduling circuitry schedules the task TA1 (col. 3, lines 35-44, *In the present example, if the pipeline 6 is executing process 8* ***when a cache miss occurs, the pipeline 6 is switched within one clock cycle to execute process*** *10 while saving the contents or states of process 8.* ***Should process 10 encounters a cache miss before the process 8 retrieves the necessary data from the main memory,*** *the pipeline 6 switches within one clock cycle to another process. Through this construction, the context of a plurality of processes 11 may be saved*), wherein the task scheduling circuitry operation does not involve instruction execution by the processor (col. 3, lines 10-26, *By state elements, the present invention refers to flip-flops and registers on the processor chip which store binary information indicative of the state of a particular process or processes. Such state elements typically comprise of register files, status bits, condition codes, and pre-fetched instructions. On the other hand, the pipeline 6 is stateless, i.e. does not store information indicative of the state of process that needs to be preserved during execution of a process. Most fast processors have at least a five-stage pipeline: they include fetch instruction, decode instruction, queue instruction for execution, execute instruction, and write result of instruction. For further reference, please see Mano, M. Morris, Computer System Architecture, (Prentice-Hall: 2nd. ed.), Chapter 22.*, and col. 4, lines 28-36, ***Applying the***

present invention to a typical processor that delivers 40 MIPS and assuming a 1% cache miss ratio and one clock cycle per instruction, the penalty for every cache miss shall be as low as one (1) clock cycle. The average number of clock cycles per instruction of the processor would be 0.01 (2) +0.99(1)=1.01. As such, the processor deliver 40/1.01=39.6 MIPS*. It follows that the present invention permits users to harness almost all the speed a fast processor can deliver*)[***emphasis added***].

Per claims, 20, and 27, further comprising third circuitry for generating a release signal indicating whether a release condition is true for releasing a task from the suspend condition, wherein the second circuitry is responsive to the release signal when the second circuitry schedules a task or tasks for execution (col. 3, lines 28-44, *FIG. 2 illustrates a typical block diagram of the state of two processes feeding the pipeline 6. It will be appreciated that a plurality of n processes can feed one pipeline, and the processes can feed each other. It is an objective of the present invention to maximize the speed of the processor by utilizing the pipeline to the fullest extent. As such, when a cache miss occurs, the pipeline shall switch from one process to another. In the present example, if the pipeline 6 is executing process 8 when a cache miss occurs, the pipeline 6 is switched within one clock cycle to execute process 10 while saving the contents or states of process 8. Should process 10 encounters a cache miss before the process 8 retrieves the necessary data from the main memory, the pipeline 6 switches within one clock cycle to another process. Through this construction, the context of a plurality of processes 11 may be saved*).

Per claims 21 and 28, the process according to claim 19, further comprising, for each task, a separate circuit for generating a signal SIG1 indicating whether the task is ready for execution,

wherein the second circuitry is responsive to one or more signals SIG1 in scheduling a task or tasks for execution (col. 3, lines 45-61, *For simple instructions,* ***pre-fetched queue transmits execution microinstructions to an execution unit 14 over a microinstruction bus 16.*** *For more complex instructions,* ***the pre-fetched queue 12 starts the micro program flow by sending signals to a micro program sequencer 18 over the bus 16.*** *An address translation unit 22 implements efficient on-chip memory management by performing virtual to physical address translation for all memory translation. When a cache miss occurs, the pre-fetched queue 12 sends a microinstruction to the address translation unit 22 over the bus 16 to fetch the address of the next process from memory. Finally, a bus control logic 26 manages the bus protocol and recognizes events such as interrupts and initialization*).

Per claim 22-29, the processor of Claim 19 wherein the second circuitry is to schedule a task or tasks for execution on each instruction executed by the processor such that whenever the processor is to execute any instruction, the second circuitry is to perform the task scheduling to schedule a task that will execute the instruction (col. 4, lines 1-26, *Note that the multiplexers in front of the plurality of state flip-flops function to preserve the context of a first process upon occurrence of a cache miss. Within one clock cycle, the pipeline can execute another process without additional idling or delay. Should the second process encounters another cache miss, the processor may return within one clock cycle to finish executing the first process if the necessary data had been retrieved from the main memory. Otherwise, the processor may begin executing a third process. It is understood that a plurality of n processes whose states are duplicated may easily be saved*).

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Maid A. Banankhah** whose voice telephone number is **(703) 308-6903**. A voice mail service is also available at this number.

All response sent to U.S. Mail should be mailed to:

Commissioner of Patent and Trademarks

Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park Two, 2021 Crystal Drive, Arlington. VA, Six Floor (Receptionist). All hand-delivered responses will be handled and entered by the docketing personnel. Please do not hand deliver responses to the Examiner.

All Formal or Official Faxes must be signed and sent to either (703) 308-9051 or (703) 308-9052. Official faxes will be handled and entered by the docketing personnel. The date of entry will correspond to the actual FAX reception date unless that date is a Saturday, Sunday, or a Federal Holiday within the District of Columbia, in which case the official date of receipt will be the next business day. The application file will be promptly forwarded to the Examiner unless the application file must be sent to another area of the office, e.g., Finance Division for fee charging, etc.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is **(703) 305-9600**.

Maid Banankhah

2/26/04

MAJID BANANKHAH
PRIMARY EXAMINER